Amendments to the Drawings:

Figures 5 and 6 have been amended as indicated below, in order to overcome the Examiner's objection that the Figures do not show the limitations of Claims 10-13. No new matter has been added. Appendix A, attached hereto, includes replacement sheets for Figures 5 and 6.

Fig. 5: blocks 506, 508, 510 and 512 have been amended to include, respectively, the pseudocode examples of micro-op instances at line 5 (506), line 8 (508), line 6 (510), and lines 10-12 (512) of Table 1.

Fig. 6: blocks 604, 608 and 610 have been amended to include, respectively, the pseudocode examples of micro-op instances at lines 4, 5, and 7 (604), line 12 (608), and lines 9 and 10 (610) of Table 2.

REMARKS and ARGUMENTS

Claims 1-61 were presented for examination. Claims 56-61 have been withdrawn from consideration. The Office Action has rejected Claims 1-6, 15, and 32-42 under 35 U.S.C. § 102(b) as being anticipated. . The Office Action has further rejected the remaining claims (7-8, 9, 10-13, 14, 16-31, 43-44, 49-51, 45-48, and 52-55) under 35 U.S.C. § 103(a). Claims 1, 14, 16, 22, 23, 24, and 32 have been amended. Reconsideration is requested in light of the amendments and the remarks and arguments set forth below.

Objections to the Drawings

The Office Action objects to the Drawings because the elements of Claims 10-13 are not shown in the figures. In particular, the Office Action claims that "[t]he drawings do not show any of these registers being used as explicit registers." (Office Action, para. 10). Figures 5 and 6 have been amended.

The amendments to Figures 5 and 6 do not add new matter but instead merely incorporate information disclosed in Tables 1-4 of the Specification.

At paragraph 43, Applicants disclose that "[d]uring micro-op generation for spills and fills, at least one embodiment of the RSE 122 makes implicit operands for spill and fill operations explicit." Such implicit operands may include special purpose application registers such as a backing store pointer register for memory stores, backing store load pointer register, and NaT collection register (RNAT). (Application, para. 43). Applicants further disclose that "the RSE 122 may generate one or more micro-operations for a register window operation that indicates such implicit operands as an explicit micro-operation operand." (*Id.*)

Thus, examples of such micro-operation instances that include RNAT, bspstore and bspload as explicit operands have been copied from Tables 1-4 into Figs. 5 and 6. No new matter has been added. The objections to the Drawings have been overcome and should be withdrawn.

Claim Rejections -35 USC § 112

The Office Action has rejected Claim 15 under 35 USC § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter. The Applicants object to the interpretation asserted by the Examiner, in that Applicants do not intend for the limitations of Claim 15 to be applied to the "other" micro-operations. The claim language of Claim 15 is supported by the Specification. For example, at paragraph 42 the Specification indicates that "the micro-ops have a fixed format 400 illustrated in Fig. 4." The format includes two source operands and one destination operand. It should be understood that the Applicants have described and claimed that the micro-ops follow a particular ***format***. The Applicants describe that this format is advantageous because "micro-ops following the fixed format 400 are easier for an out-of-order processor ... to rename, schedule, and execute ..." (Application, para. 42).

Applicants assume that, by the following statement, the Examiner is basing the rejection on the sample micro-operations set forth in Tables 1-4: "The load and store instructions in the specification do not support having a single destination register and two source registers." (Office Action, page 4). The Examiner seems to be confusing the idea of an instruction ***format*** with the ***instance*** of a particular instruction that follows the format. Tables 1 – 4 clearly show ***instances*** of instructions following a 1-destination and two-source ***format***, in which the second source field is null. All other portions of the Specification, Drawings, and claims support the

idea that the micro-ops are of the format 400 illustrated in Fig. 4. The rejection of Claim 15 should be withdrawn.

The Office Action has also rejected Claim 24 for lack of antecedent basis. Claim 24 has been amended to correct this error; the rejection has been overcome and should be withdrawn.

Claim Rejections -35 USC §§ 102(e) and 103(a)

The Office Action has rejected Claims 1-6, 15, and 32-42 under 35 U.S.C. § 102(b) as being anticipated by a publication of a formerly pending U.S. Patent Application to Bui, 2002/0056024 (hereinafter "Bui"). (Bui issued as U.S. Patent No. 5,941,977 on August 24, 1999). Of these claims, Claims 1 and 32 are independent claims. However, the Office Action has failed to make a prima facie case of anticipation for the claims as amended, and such rejections should be withdrawn.

The Office Action has rejected Claims 7-8, 9, 10-13, 14, 16-31, 43-44, 49-51, 45-48, and 52-55 under 35 U.S.C. § 103(a). Of particular relevance to this response, Claims 14, 16, 22, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bui, in light of U.S. Pat. No. 5,941,977 to Panwar et al. (hereinafter "Panwar").

Bui generally discloses a register stack engine (RSE) mechanism that operates concurrently with a backing store memory (Bui, page 1, paragraph 14). Bui does not disclose, suggest or teach the ***out-of-order*** **scheduling** or ***out-of-order*** **execution** of micro-ops for register window operations such as spills and fills.

Panwar is directed to a method for speculatively converting logical addresses to physical addresses (Panwar, Abstract). Panwar generally discloses a scheduler (ISU) at Fig. 2, and describes that renamed instructions may be registered for execution by the ISU (Col. 6, lines 19-

20). However, the **Panwar scheduler does not insert micro-operations for a register window micro-operation into an execution pipeline or schedule such micro-ops, but instead handles spills and fills via trap and privileged software**.

The scheme disclosed and claimed by Applicants is directed toward the problem that "it would be desirable for spill and fill operations to accommodate structures that support out-of-order execution, such as out-of-order rename units and out-of-order schedulers ..." (Application, paragraph 4, pages 2-3).

Although Claims 1 and 32 were rejected under 35 U.S.C. § 102 as being anticipated by Bui, each of these claims has been amended herein to incorporate limitations from a claim that was rejected under 35 U.S.C. §103. "[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). The Office Action admits that these elements that have been amended into Claims 1 and 32 are not shown in Bui (see discussion below of Claim 14 rejection). Thus, the 102 rejections for Claims 1 and 32 must be withdrawn in light of the current amendments.

Accordingly, all independent claims, as amended, are discussed below in connection with rejections set forth in the Office Action concerning 35 U.S.C. § 103. The legal requirements for a prima facie case of obviousness are clear. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has not met this burden with respect to amended Claims 1, 16, 24 or 32.

Claims 1 and 16. Claims 1 and 16 are not anticipated by Bui. For example, Claim 1 recites, in part, "the scheduler is to concurrently consider the one or more micro-operations as well as other micro-operations in an out-of-order scheduling scheme " (Claim 1, in part). This element, formerly in Claim 14, has been incorporated into Claim 1 by amendment.

Claim 16 recites, in part, "the scheduler is to perform out-of-order scheduling for a set of micro-operations, wherein the set of micro-operations includes the one or more micro-operations to cause a register stack operation as well as other micro-operations" (Claim 16, in part). This element, formerly in Claim 22, has been incorporated into Claim 16 by amendment.

Bui does not teach, suggest or disclose the quoted limitations of Claims 1 and 16. The Office Action admits this ("Bui failed to teach a scheduler to schedule the micro-operations for execution and wherein the scheduler is to concurrently consider the register window operation micro-operations as well as other micro-operations in an out-of-order scheduling scheme") at page 14, paragraph 50 of the Office Action.

The Office Action rejects Claims 14 and 22 on the same basis, so they will both be discussed below in connection with the rejection of Claim 14.

The Office Action states that these elements (formerly of Claims 14 and 22) are found at Figure 2 element 206 and column 6, lines 19-50 of U.S. Pat. No. 5,941,977 to Panwar et al. (hereinafter "Panwar"). However, this element is not shown in Panwar.

It is true that Fig. 2 shows an ISU, which is an instruction scheduling unit (see Col. 6, line 12-13). And, it is also true that the operation of the ISU is further explained at column 6, lines

19-50 of Panwar. However, the **Panwar scheduler does not schedule micro-operations for a register window micro-operation**.

Instead of inserting register window operation micro-ops into the execution pipeline such that the micro-ops can be handled by an out-of-order scheduler, the Panwar scheme handles spills and fills as traps that invoke privileged software. (See, e.g., Panwar, Col. 10, line 34: "windowing traps such as window spill or fill exception"). Panwar explains that spills and fills are handled by "a spill trap or exception that allows privileged software to save the occupied register in memory" and "a fill or trap exception that allows privileged software to load the window registers from memory." (Panwar, Col. 7, line 67 – Col. 8, line 7). **Panwar's handling of register window spills and fills as exceptions or traps handled by software code does not teach, disclose or suggest the handling of register window operation micro-ops by an out-of-order scheduler**.

The Office Action states that Panwar discloses a scheduler to schedule the micro-operations for execution. This is just wrong. Panwar does not schedule micro-operations for register window operations. Instead, they are handled by exception. Thus, neither reference shows the cited elements. A combination of the references cannot show the elements, if neither reference shows them.

The cited portions of Bui are simply not sufficient to make a prima facie case of obviousness regarding Claims 1 and 16. Similarly, Panwar also fails to make a prima facie case of anticipation. Panwar and Bui each fail to show a scheduler that is "to concurrently consider the one or more micro-operations as well as other micro-operations in an out-of-order scheduling scheme" (Claim 1, in part) and also fail to show a scheduler that is "to perform out-of-order scheduling for a set of micro-operations, wherein the set of micro-operations includes the one or

more micro-operations to cause a register stack operation as well as other micro-operations (Claim 16, in part).

Because neither reference shows these elements, a combination of the references doesn't show them either. Thus, neither a prima facie case of anticipation nor a prima facie case of obviousness have been made out with respect to Claims 1 and 16.

For at least the foregoing reasons, a prima facie case of anticipation has not been made with respect to Claim 1. Claim 1 is therefore allowable and the rejections must be withdrawn based on failure to make a prima facie case of anticipation. In addition, Claims 2-15, which depend from Claim 1 are also allowable.

For at least the foregoing reasons, a prima facie case of anticipation has not been made with respect to Claim 16. Claim 16 is therefore allowable and the rejections must be withdrawn based on failure to make a prima facie case of anticipation. In addition, Claims 17-23, which depend from Claim 16 are also allowable.

Claims 24 and 32.

Claim 24 recites, in part, "performing an out-of-order rename stage for each of one or more micro-operations ..." (Claim 24, in part).

Amended Claim 32 recites, in part, "where the pipeline includes an out-of-order rename stage for each of the one or more micro-operations." (amended Claim 32, in part).

The Office Action admits that Bui fails to disclose these limitations: "Bui failed to teach performing an out-of-order rename stage for each of the one or more micro-operations." (Office Action, page 17, para. 59) However, the Office Action asserts that this element is shown in

Panwar, claiming that "Panwar disclosed performing an out-of-order rename stage for each of the one or more micro-operations." (*Id.*) This interpretation of Panwar is mistaken.

Panwar does not disclose this limitation. Instead of inserting micro-operations for spills and fills into the execution pipeline, the Panwar scheme handles overflows and underflows of the register window with a trap that his handled by privileged software code. **In Panwar, there are no micro-operations inserted into the pipeline, so they cannot be renamed in the execution pipeline**.

Thus, there is simply no teaching whatsoever in Panwar toward "performing an out-of-order rename stage for each of the one or more micro-operations". For at least the foregoing reasons, a prima facie case of anticipation has not been made with respect to Claims 24 and 32.

Claim 24 is therefore allowable and the rejections must be withdrawn based on failure to make a prima facie case of anticipation. In addition, Claims 25-31, which depend from Claim 24, are also allowable for at least the foregoing reasons.

In addition, Claim 32 is therefore allowable and the rejections must be withdrawn based on failure to make a prima facie case of anticipation. In addition, Claims 33-51, which depend from Claim 32, are also allowable for at least the foregoing reasons.

In conclusion, Applicants respectfully submit that the applicable rejections have been overcome and must all be withdrawn. For at least the foregoing reasons, independent Claims 1, 16, 24, and 32 are allowable. In addition, all claims that depend from these independent claims are also allowable. Applicants reserve all rights with respect to the application of the doctrine equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this

case. If the Examiner feels that an interview would help to resolve any remaining issues in the case, the Examiner is invited to contact Shireen Bacon of Intel, at (512) 732-3917.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

Dated: October 2, 2006

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APPENDIX A

Fig. 5 Replacement Sheet

Fig. 6 Replacement Sheet